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Thin germanium oxynitride gate dielectric for germanium-based devices

FIELD OF THE INVENTION

The present invention relates to electronic devices and systems. In particular it relates to a method of producing a germanium oxynitride layer for use as a thin gate dielectric.

BACKGROUND OF THE INVENTION

Today's integrated circuits include a vast number of devices. Smaller devices are key to enhance performance and to improve reliability. As MOS (Metal Oxide Semiconductor Field- Effect- Transistor, a name with historic connotations meaning in general an insulated gate Field- Effect- Transistor) devices are being scaled down, the technology becomes more complex and new methods are needed to maintain the expected performance enhancement from one generation of devices to the next.

SUMMARY OF THE INVENTION

Gate dielectrics is one of the main problems for MOS field effect device scaling. This is true for both conventional silicon devices and more advanced (e.g. SiGe, Ge) devices.

In Ge-based devices, the situation is quite complicated. The term "Ge-based" typically refers to SiGe compounds, where the Ge concentration is over about 30-40%. The term Ge-based also includes an essentially pure Ge material. So far no reliable high-quality gate dielectric has been found for Ge based materials. Germanium oxide is of poor quality and is soluble in water. Binary metal oxides (e.g. ZrO_2, HfO_2) show ~ 40% electron mobility degradation when used as gate dielectrics. Germanium oxynitride quality and scaling potential up to now was thought to be inferior to the SiO_2/Si system.

Ge-based devices are a higher-performance alternative to conventional Si-based devices due to their better carrier mobility, especially for holes. Of all gate insulators on Ge substrates explored and reported so far, germanium oxynitride shows best potential performance. However, the rate of thermal oxidation/oxynitridation of Ge is much faster than that of Si. This makes it difficult to grow thin germanium oxynitride films with good process control, and/or with an equivalent oxide thickness (EOT) of below about 6nm. (Since the quintessential gate dielectric material is SiO_2, this material stands a the standard for comparison. Since the dielectric constant of germanium oxynitride [about 6 to 9] differs form that of SiO_2, the meaningful value as far as thickness is concerned is an equivalent thickness in SiO_2. This equivalence refers to capacitance, meaning the thickness of such an SiO_2 layer which has the same capacitance per unit area as the germanium oxynitride layer.)

The present invention offers a solution for the problem of growing a thin germanium oxynitride layer in a controlled manner. The solution involves using a two

step process. The first step being incorporating a first concentration of nitrogen into a surface layer underneath a first surface of the Ge-based material. This nitrogen-rich region acts as a diffusion/reaction barrier that controls the germanium oxidation/oxynitridation rate in a second, oxidation step. Such a control allows one to grow ultrathin germanium oxynitrides in a governable, reproducible manner. The thin germanium oxynitride gate dielectric allows for improved properties and higher performance in Ge-based field effect devices.

The method of the present invention offers two independent controls of the dielectric formation. Firstly, the initial step defines nitrogen incorporation into the surface/subsurface region of Ge-base material substrate, and hence its diffusion barrier "power", and dielectric constant. Secondly, the subsequent oxidation step controls final thickness of the germanium oxynitride film.

Accordingly it an objective of the present invention to teach a method of producing a thin, below 6nm, preferably below 5nm of EOT, good quality germanium oxynitride insulator layers on Ge-based materials.

It is also an object of the invention to teach a method for fabricating Ge-based field effect devices which contain the good quality germanium oxynitride insulator layers as gate dielectrics.

It is a further object of the present invention to teach processors which comprise chips containing such a Ge-based field effect device having preferably below 6nm of EOT, good quality germanium oxynitride gate insulator layers on Ge-based materials.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other features of the present invention will become apparent from the accompanying detailed description and drawings, wherein:

Fig. 1 shows nitrogen incorporation steps of the method in representative embodiments;

Fig. 2 shows a plot of nitrogen incorporation vs. thermal conditions in the execution of the nitrogen incorporation step;

Fig. 3 shows the oxidation step completing the production of a thin germanium oxynitride layer;

Fig. 4 shows plots of the thickness and EOT of the thin germanium oxynitride layer vs the conditions of the oxygen ambient exposure step;

Fig. 5 shows a schematic cross sectional view of a Ge-based field effect device having a thin germanium oxynitride gate dielectric; and

Fig. 6 shows a symbolic view of a high performance processor containing at least one chip which contains a Ge-based field effect device having a thin germanium oxynitride gate dielectric.

DETAILED DESCRIPTION OF THE INVENTION

In the fabrication of high performance Ge-based field effect devices the processing steps that preceded the production of the gate dielectric are known in the art. These steps, such as device isolation, dopant well formation, etc., are assumed to have been completed before commencing the steps of the present invention. However, before the disclosed method steps can take place to produce an the thin germanium oxynitride layer, a surface, referred to as a first surface, of the Ge based material, generally a wafer, the one which will be the recipient of the gate dielectric, has to be properly cleaned. In a representative embodiment such cleaning steps can include, but are not limited to, at least one cycle of oxidation and germanium oxide removal. The oxidation is preferably performed in H_20_2 solutions, while oxide removal is accomplished by HF, or HCl, or their mixtures. After the cleaning step the first surface of the Ge based material, which is host to the devices, is ready for a step by which a first concentration of nitrogen will become incorporated into a surface layer underneath the first surface.

Fig. 1 shows a nitrogen incorporation steps of the method in representative embodiments. Fig. 1A shows an embodiment wherein the nitrogen incorporation is carried out by subjecting the first surface 5 of the Ge-based body 160, typically the surface of a Ge-based material wafer, to a nitrogen containing gas under thermal, or plasma conditions. The reactive nitrogen containing gas in a representative embodiment is NH_3. In alternate embodiments this nitrogen containing reagent may also be NO or

N_2O. In further alternate embodiments one can use various combinations of the gases NH_3, NO, or N_2O. All of these species can be sources of atomic nitrogen under the proper circumstances. In each case these active components can be mixed in with inert components, or carrier gases, such as N_2, Ar, He, etc..

The thermal conditions for this chemical nitrogen incorporation step can be between 450°C and 700°C applied for between 1 second and 300 seconds. The temperature typically is applied by rapid thermal annealing techniques, well known in the art. Conditions for this step in a representative embodiment can be: NH_3 active gas at 600°C for 30 seconds. Depending on the conditions, the resulting nitridated thin layer 90 characteristically is between about 0.5nm and 1.5nm thick. This layer 90 incorporates a first concentration of nitrogen, which first concentration has an integrated value giving a surface density of incorporated nitrogen between about 1E14 per cm^2 and 3E15 per cm^2.

The nitrogen incorporation step can also be performed by the use of plasma nitridation. In this case, a first surface of the Ge-based surface is exposed to a low energy nitrogen containing plasma. It can be done in a direct plasma mode or by remote (downstream) plasma nitridation. Plasma power can be varied in the about 25W - 1000W range, exposure preferably is between 1sec and 300 sec. The sample temperature during plasma exposure is preferred to be from about room temperature to 500°C. N_2, NH_3 and N_2O gates can be used in plasma reactors as N source.

Fig. 1B schematically shows the step of nitrogen incorporation when this step is carried out by ion implanting 70 a nitrogen dose into the first surface 5 on the Ge-based

material body 160. The implantation energy should be low, typically between 0.5KeV and 10keV. In this manner the N ends up located close to the first surface 5 in a layer 90. Alternatively, instead of using such low implant energy, but to assure that the N will be in the thin layer 90, the ion implantation can be performed through a thin, 10nm to 30nm, screen layer. Such screening techniques are known in the art. The screen layer in an exemplary embodiment being, for instance, deposited $Si0_2$, which after the implantation can be chemically removed. The implant dose of N can typically be between about 1E15 per cm^2 and 2E16 per cm^2.

Fig. 2 shows a plot of characteristic nitrogen incorporation vs. thermal conditions in the execution of the N incorporation step, as the concentration is being measured by nuclear reaction analysis. On the vertical axis the integrated concentration in the layer 90 is shown against the temperature of reaction when NH_3 was the reagent gas, during a 30 sec exposure.

Independently, whether the nitrogen incorporation step is carried out by subjecting the first surface 5 to a nitrogen containing gas under thermal conditions or plasma conditions, or by N ion implantation, the amount of nitrogen, introduced in the nitrogen incorporation step governs the oxidation rate during the next, the oxidation step. With the trend of more nitrogen providing more slow reoxidation kinetics, and therefore thinner films.

Fig. 3 shows the oxidation step which completes the production of the thin a germanium oxynitride layer. This is a second step in the invention, when the nitrogen

containing layer controls the oxidation rate of the Ge-based material 160 as the first surface 5 is exposed to an oxygen ambient under thermal, or plasma conditions. The thin surface layer incorporating nitrogen 90 is regulating production of the oxynitride layer 100, while layer 90 itself is also transformed into the oxynitride layer 100.

The oxygen ambient in a representative embodiment contains as reactive species O_2, O_3, H_2O, NO, N_2O since they can be sources of atomic oxygen. Combinations of these gases can also be used. Typically the reactive gases can be mixed in with inert components, such as N2, Ar, He, etc.. That the oxidation step can also be performed in nitrogen containing gases, such as, N_2O, NO is due to the fact that they tend to decompose at high-temperatures releasing atomic oxygen. Similarly, oxidation can be carried out by wet oxidation using H2O vapor mixed in a carrier inert gas. The thermal ambient in this step is typically a temperature between 500°C and 700°C, applied for between 1 minute and 30 minutes. After finishing with the oxygen exposure step the germanium oxynitride layer is ready as the gate dielectric, and one can proceed with further processing of devices in a standard manner.

The oxidation step can also be performed by the use of plasma oxidation. In this case, the first surface 5 with the nitrogen containing layer 90 underneath is exposed to a low energy oxygen containing plasma. This can be done in a direct plasma mode or by remote (downstream) plasma oxidation. Plasma power can be varied in the about 25W - 1000W range, exposure preferably is between 1sec and 300 sec. The sample temperature during plasma exposure is preferred to be from about room temperature to 500°C. The

same oxygen containing species can be used as with the thermal oxidation.

Fig. 4 shows plots of the thickness and of the EOT of the thin germanium oxynitride layer 100 vs the conditions of the oxygen ambient exposing step, when the nitrogen incorporation step involved NH_3 exposure at 600°C for 5 minutes. Since the quintessential gate dielectric material is SiO_2 this material stands a the standard comparison. Since the dielectric constant of germanium oxynitride differs form that of SiO_2, it is useful to not only give the thickness of the thin germanium oxynitride layer 100, but also give equivalent thickness in SiO_2. The equivalence means the thickness of such an SiO_2 layer which has the same capacitance per unit area. Thus in Fig. 4 the EOT values are the results of standard capacitance versus voltage measurements. Fig. 4 shows how sensitively the thickness of the germanium oxynitride can be controlled, and that the EOT of the germanium oxynitride layer is tuned even in the unprecedented, below 5nm range, by controlling the thermal budget during the oxygen exposure step.

This invention can thus produce germanium oxynitride layers that have less than about 10nm of EOT. A preferred range of germanium oxynitride gate dielectric for high performance devices is below 6nm of EOT, preferably having a range between 0.5nm and 5nm of EOT.

When the Ge-based material is actually essentially pure Ge, the invention is particularly significant, since pure Ge devices can potentially deliver the best performance.

It is emphasized that the present method offers an additional process flexibility,

namely to grow multiple, for example dual, oxynitride dielectric thicknesses for different devices/applications on the same wafer by incorporating different amounts of nitrogen in differing parts of the wafer. The first surface 5, would have at least two differing locations, where the nitrogen incorporation step is carried out in manners to yield differing first concentrations of the incorporated nitrogen. Accordingly, the produced, final oxynitride layers on the at least two locations end up having differing EOT.

Fig. 5 shows a schematic cross sectional view of a Ge-based field effect device 10 having a thin germanium oxynitride layer 100 gate dielectric, preferably having an equivalent oxide thickness of less than 5nm. The gate dielectric germanium oxynitride 100 is an insulator, separating a conductive gate 110 from a Ge-based body 160.

Germanium oxynitride, in general, has a high dielectric constant, which means over approximately 4, which can result in germanium oxynitride having a high barrier, namely exhibiting high resistance, against charge tunneling. As the thickness of gate dielectrics is decreasing in order to increase the gate-to-channel capacitance, resistance against charge tunneling across the gate dielectric is an important issue. The standard gate dielectric material SiO_2 (dielectric constant of 3.9), does have such problems. Since the dielectric constant of germanium oxynitride is larger than that of SiO_2, a germanium oxynitride layer which has the same capacitance per unit area as a SiO_2 layer is thicker than the SiO_2 layer. Since resistance against tunneling depends exponentially on layer thickness, the germanium oxynitride layer will tend to be the more charge penetration resistant.

Fig. 5 depicting a Ge-based, or in a representative embodiment pure Ge, field effect device is almost symbolic, in that it is meant to represent any kind of field effect device. The only common denominator of such devices is that the device current is controlled by a gate 110 acting by its field across an insulator, the so called gate dielectric 100. Accordingly, every field effect device has a (at least one) gate, and a gate insulator.

Fig. 5 depicts schematically an MOS field effect device, with the source/drain regions 150, device body 160. The body, can be bulk, as shown on Fig. 5, or it can be a thin film on an insulator. The channel can be a single one, or multiple one, as on double gated, or FINFET devices. The basic material of the device can be of a wide variety. The body can be a Ge compound, or consisting of essentially pure Ge.

In a representative embodiment the Ge-based field effect device is a Ge MOS. In a further representative embodiment the Ge-based field effect device has a germanium oxynitride layer gate dielectric which preferably has an EOT range between 0.5nm and 5nm.

Fig. 6 shows a symbolic view of a high performance processor 900 containing at least one chip 901 which contains a Ge-based field effect device10 having a thin germanium oxynitride gate dielectric, which has an EOT of less than 5nm. The processor 900 can be any processor which can benefit from the germanium oxynitride gate dielectric Ge-based field effect device. These devices can form part of the processor in their multitude on one or more chips 901. Representative embodiments of processors manufactured with the thin germanium oxynitride gate dielectric Ge-based field effect

devices are digital processors, typically found in the central processing complex of computers; mixed digital/analog processors, which benefit significantly from the high mobility of the carriers in the germanium oxynitride gate dielectric field effect devices; and in general any communication processor, such as modules connecting memories to processors, routers, radar systems, high performance video-telephony, game modules, and others.

Many modifications and variations of the present invention are possible in light of the above teachings, and could be apparent for those skilled in the art. The scope of the invention is defined by the appended claims.